**Project 10: Advanced Thin Silicon High Efficiency Device Integrations**
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## Motivation

Improvements in Silicon solar cell designs and advanced fabrication techniques have resulted in laboratory efficiencies of almost 25% using 300 micron thick Silicon wafers while in production, efficiencies on Si PV cells exceeding 22% using approximately 150-200 micron thickness have been reported[1]. Notwithstanding the attainment of higher efficiencies, the cost of Silicon solar cells remains high, in large measure due to the cost of crystalline Silicon (c-Si). Today, the cost of Silicon accounts for about 75% of the cost of each cell and approximately 50% of the cost of a module [2,3,4,5]. One approach towards significantly lowering the cost of Silicon solar cells is to significantly, by as much as a factor of 10, decrease the thickness of the crystalline Si (c-Si) wafers used in the cells while maintaining the conversion efficiencies near the 20% level. In fact, it has been reported that with wafers of thickness less than 50µm, c-Si PV cells can still achieve efficiencies greater than 20% [6]. However, the principal barrier to thin c-Si PV cells (<50µm thickness) being thoroughly researched and developed has been the lack of a commercially viable option for the production of thin Silicon wafers without the large kerf losses associated with the traditional wire saw cutting method. Within the last year, a new kerf-free technique employing a high energy proton beam to successfully cleave wafers as thin as 20µm has been reported[7]. With the potential of commercial availability of ultra-thin c-Si wafers becoming a reality, there is now significant impetus to research and develop high efficiency thin Silicon photovoltaics with the ultimate target of attaining module costs of less than US$1/Watt-peak.

The use of thin wafers also has the additional benefit of mitigating photo-induced degradation in the Silicon solar cells. Typical 300 µm Czochralksi (Cz) c-Si solar cells suffer a 3-5% decline in output power after a few hours of sunlight exposure[8]. This photo-degradation owes to an increase in the density of recombination centres, and associated decrease in carrier diffusion lengths, due to the formation of boron-oxygen complexes in the p-type region. A reduction in wafer thickness correspondingly reduces the distance that free carriers need to traverse to reach the cell contacts and accordingly the effect of decreased diffusion lengths is mitigated. As an example, it has been shown that c-Si PV cells using Cz wafers with thicknesses of 100µm exhibit less than 1% photo-induced degradation[9].

## Background

Several studies have been carried out to examine the potential of ultra-thin wafers for c-Si PV cells. Munzer *et al* found that when a standard p-n junction c-Si cell is fabricated without a back-surface field (BSF), a built-in field designed to reflect minority carriers from the back surface, the efficiency of the cell strongly decreases with decreasing wafer thickness; however, with a well-designed BSF the cell efficiency actually increases with decreasing thickness[10]. The stabilized efficiencies (after photo-induced degradation) measured on cells with a BSF were 15.9%, 16.0%, and 16.2%, for thicknesses of 200µm, 150µm, and 100µm, respectively. The increase in efficiency with decreasing thicknesses was attributed to a decrease in photo-induced degradation.

Upadhyaya *et al* modeled the effect of reduced wafer thickness on multicrystalline (mc) Si PV cells[11]. They found that if effective light trapping and surface passivation schemes are implemented, the efficiency of a cell using a 100µm thick wafer would be 18% compared with an efficiency of 16.9% for the identical cell using a 280µm thick wafer. Recently, Glunz reported efficiencies of 21.2% and 20.2% for c-Si PV cells on Cz wafers with thicknesses of 75µm and 37µm, respectively[12]. These cells employed surface passivation on both the emitter and the base and had rear point contacts on the base.

## Technical Challenges

There are several technical challenges associated with developing commercially-viable c-Si PV cells using ultra-thin wafers. Mechanically, these ultra-thin wafers are more prone to breaking and warping, requiring special handling and processing. Thermal stresses associated with high temperature (>600°C) processing ought to be avoided. Typical cell interconnection techniques such as using 150µm thick copper ribbons need to be adapted to avoid mechanical stresses on the wafer[13]. In addition to these mechanical issues, ultra-thin wafers require advanced light confinement techniques so as to maintain high photon absorptivity; for example, Silicon absorption lengths are 10µm and ~1mm for $\lambda$=800nm and $\lambda$=1100nm, respectively.

Perhaps the greatest technical challenge in using ultra-thin wafers is the need for very low surface recombination. In c-Si, the majority of the defects lie on the front and back surfaces resulting in a corresponding increase in the surface recombination velocity and accordingly a reduction in the conversion efficiency of the cell. As the thickness of the cell is reduced, significant photon absorption occurs closer to the back surface of the cell leading to an increase in the density of minority carriers near the back surface. The combination of a high density of surface recombination centres and the increased density of minority carriers at the back surface leads to a decrease in cell performance. One approach to lowering the surface recombination is to create a back-surface field (BSF) which acts as a minority carrier mirror. Common approaches to implementing BSFs are through p+p (n+n) junctions in p- (n-) type wafers, typically achieved through high temperature boron (phosphorus) diffusion or aluminum alloying. While these techniques are amenable to wafers of the order of 200 µm thickness, significant wafer warping occurs in ultra-thin wafers (<50µm)[14], hence requiring research into simple and production-amenable, inexpensive, low-temperature alternatives. Another approach to reducing rear surface recombination is the use of point contacts on the back-surface interspersed amid a passivating thin film dielectric. A common approach is $SiO_2$ films grown at high temperatures (~1000°C), which are also not suitable for ultra-thin wafers[15] , hence requiring research into alternative passivating films deposited at lower temperatures.

**Proposed Research**

The long-term objective of the proposed research is to develop commercially-viable, low-cost, c-Si PV cells on ultra-thin wafers (20µm-50µm) with greater than 20% conversion efficiency. In order to advance this objective, three sub-projects involving inter-university collaborations among researchers in the Network are presented below.

*1. Passivation and Generation of BSF on Ultra-Thin c-Si Wafers*

The objective of this sub-project is to investigate a range of candidate low-temperature processed thin film materials amenable to high quality interfacial passivation and/or the formation of a back surface field. Candidate thin film materials that will be investigated include hydrogenated amorphous Silicon alloys and hydrogenated amorphous carbon alloys. Potential compounds include hydrogenated amorphous Silicon carbide (a-Si:C:H), hydrogenated amorphous silicon oxide (a-Si:O:H), hydrogenate amorphous Silicon nitride a-Si:N:H, hydrogenated amorphous carbon (a-C:H) and hydrogenated amorphous carbon nitride (a-C:N:H); in this context, quaternary compounds may also be investigated. Additional dopant impurities, such as boron and phosphorus, may be introduced into these films to further investigate the efficacy of BSF layers. Other candidate oxide based materials that may be investigated include aluminum oxide and nickel oxide systems[16,17,18,19]. As a reference, thermally grown Silicon oxide passivation on ultra-thin wafers will also be investigated. In this context, front surface fields will also be investigated; front surface fields being appropriate in advanced cell designs such as the back amorphous-crystalline Silicon heterojunction (BACH) cells.

The above described candidate thin film compounds will be deposited using the new tuneable plasma enhanced chemical vapour deposition facility in the Advanced Photovoltaics and Devices Laboratory at the U. of Toronto. The deposition system affords dc, dc saddle-field, rf, and dc-rf augmented electrode configurations along with *in situ* deposition and diagnostic tools that allow for the growth of controlled, high quality films. Some of the *in situ* features of the system include: tunable electrode spacing, ellipsometry for growth characterization, and ion-mass spectroscopy for characterization of species arriving at the growth surface, and Langmuir probe for plasma characterization. The films will be examined for their passivating quality using microwave photoconductive decay, quasi-steady state photoconductance and capacitance-voltage analysis; for their optical properties using spectroscopic ellipsometry and UV-Visible spectroscopy; and for their structural properties using various advanced electron microscopy techniques.

*2. Advanced Light-Trapping Techniques*

Alternative light confinement techniques need to be researched to achieve high photon absorptivity in ultra-thin wafers, as standard techniques such as alkaline texturization may not be easily applicable on ultra-thin wafers (for example, owing to handling limitations; and, recently produced ultra-thin wafers are of <111> orientation[20] ). Yoblanovitch *et al*. have shown that in a thin homogeneous film of index of refraction n the optical path length can be enhanced at most to a value of $4n^2$ [21]. This involves attaining perfect random scattering on the incident surface and a lossless back reflector. When applied to Silicon, this suggests a maximum path-length enhancement of ~50, yet in reality the actual value is closer to 10. Much larger path-length enhancement factors, on the order of $10^3$ to $10^4$, are required to effectively absorb near-bandgap photons for ultra-thin wafers. An alternative approach to texturing is light localization through the application of photonic crystals[22]. Photonic crystals are periodic dielectric structures that affect the behaviour of electromagnetic waves similar to periodic potentials in semiconductor lattices that affect the behaviour of electron waves. It is expected[23] that integration of photonic crystal constructs into photovoltaic devices can result in optical path length enhancements of greater than 10,000.

The objective of this sub-project will be to investigate photonic crystal constructs that can be integrated with Silicon based photovoltaic devices. Specifically, the experimental investigation will focus on the development of 1-dimensional photonic crystals from dielectric and transparent conducting materials whereby these structures can be employed as optical and optical-electrical elements, respectively, in devices. Candidate material systems include opaline photonic crystals based on silica monodispersed spheres, transparent conducting oxide nano-spheres, transparent conducting films, and other dielectric films having a range of optical and electrical properties. Fabrication and characterization of these structures will occur within the Nanochemistry and ECTI Laboratories at the U. of Toronto and at McMaster. The photonic crystal constructs will be studied for their optoelectronic and structural properties using a range of diagnostics including UV-VIS-NIR ellipsometry, conductivity apparatus, and microscopy techniques. The effect of the photonic crystal structures on near-bandgap photon absorption will be measured through internal and external quantum efficiency measurements.

*3. Integration with High-Efficiency Advanced Cell Concepts*

The objective of this sub-project is to undertake the integration of the various high efficiency techniques/processes developed and advanced cell-concepts amenable to commercially-viable solar cells fabricated from ultra-thin crystalline Silicon wafers. At the time of writing, four candidate cell structures have been identified for potential integration within ultra-thin c-Si wafers: (a) bi-facial amorphous-crystalline Silicon heterojunction device; (b) back amorphous-crystalline Silicon heterojunction device; (c) rapid thermal annealing assisted, ion-implanted crystalline Silicon homojunction; and (d) III-V compound semiconductors on Silicon. The focus of the research will be coupling passivation and light-trapping functionality into these cell concepts, and developing fabrication methods for these cell concepts (for example, low mechanical stress preparations) suitable for ultra-thin wafers.

The fabrication and integration of the above described cells will occur at both the U. of Toronto and McMaster, availing appropriate heterojunction, ion implantation and III-V preparation facilities at the two institutes. Characterization of these devices will also occur at both universities.

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